Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Claims 1-8. (Canceled)

9. (Previously presented) The integrated circuit synchronous read channel of claim 14 further comprising digital pulse shaping filter circuitry ~~for modification of~~that operates to modify the digitized read signals prior to receipt thereof by at least one of (i) the sequence detector, (ii) the digital peak detector and (iii) the timing recovery circuit.

10. (Currently amended) An integrated circuit synchronous read channel for receiving digitized read signals representing digitized samples of a read signal of a magnetic storage device and recovering digital data represented thereby, the integrated circuit comprising:

a digital peak detector ~~for detecting~~that operates to detect characteristics of the digitized read signals indicative of storage media transitions;

timing recovery circuitry responsive to the digitized read signals and ~~the~~ an output of the digital peak detector ~~to provide~~that operates to provide a timing control signal for controlling the timing of digitized samples of the read signal

a sequence detector responsive to the digitized read signals ~~for receiving~~that operates to receive a stream of the digitized read signals and ~~determining~~ determine a corresponding sequence of binary digital signals likely to be represented thereby;

an RLL (d,k) decoder ~~for providing~~that operates to provide a run length limited decoded output by decoding the sequence of binary digital signals from the sequence detector, or to provide a run length limited decoded output by decoding a sequence of binary digital signals from the digital peak detector;

digital pulse shaping filter circuitry ~~for modification of~~that operates to modify the digitized read signals prior to receipt thereof by at least one of (i) the sequence detector, (ii) the digital peak detector and (iii) the timing recovery ~~circuit~~circuitry; and

delay ~~means~~circuitry ~~for delaying~~that operates to delay the coupling of the digitized read signals to the digital peak detector or the timing recovery ~~circuit~~ circuitry

to match the delay of the coupling of the digitized read signals to the timing recovery circuitry or the digital peak detector, respectively, imposed by the digital pulse shaping filter circuitry.

11. (Currently amended) The integrated circuit synchronous read channel of claim 10 wherein the digital pulse shaping filter circuitry ~~includes~~ comprises variable filter parameters.

12. (Currently amended) The integrated circuit synchronous read channel of claim 10 wherein the digital pulse shaping filter circuitry ~~includes~~ comprises programmable filter parameters.

13. (Currently amended) The integrated circuit synchronous read channel of claim 10 further comprising spectrum smoothing filter circuitry ~~for filtering~~that operates to filter the digitized read signals prior to processing by the sequence detector.

14. (Currently amended) An integrated circuit synchronous read channel for receiving digitized read signals representing digitized samples of a read signal of a magnetic storage device and recovering digital data represented thereby comprising:

a digital peak detector ~~for detecting~~that operates to detect characteristics of the digitized read signals indicative of storage media transitions;

timing recovery circuitry responsive to the digitized read signals and ~~the~~ an output of the digital peak detector ~~to provide~~that operates to provide a timing control signal for controlling the timing of digitized samples of the read signal

a sequence detector responsive to the digitized read signals ~~for receiving~~that operates to receive a stream of the digitized read signals and ~~determining~~ determine a corresponding sequence of binary digital signals likely to be represented thereby; and

an RLL (d,k) decoder ~~for providing~~that operates to provide a run length limited decoded output by decoding the sequence of binary digital signals from the sequence detector, or to provide a run length limited decoded output by decoding a sequence of binary digital signals from the digital peak detector,

wherein the sequence detector ~~processes~~ is operable to process two digitized read

signals at a time, the two digitized read signals representing digitized samples of a read signal of a magnetic storage device during two successive channel bit times.

15. (Currently Amended) The integrated circuit synchronous read channel of claim 10, wherein the sequence detector ~~allows~~ operates to allow selection between center and side sampling of the digitized read signals.

16. (Currently Amended) The integrated circuit synchronous read channel of claim 10, wherein the sequence detector ~~accommodates~~ operates to accommodate pulse asymmetry in the digitized read signals.

17. (Previously presented) The integrated circuit synchronous read channel of claim 10, wherein the sequence detector is a partial response sequence detector.

18. (Previously presented) The integrated circuit synchronous read channel of claim 10, wherein the timing recovery circuit operates in at least one of an acquisition mode and a tracking mode.

19. (Previously presented) The integrated circuit synchronous read channel of claim 10, wherein the timing recovery circuit is programmable.

20. (Currently Amended) The integrated circuit synchronous read channel of claim 10, wherein the timing recovery circuit ~~computes~~ operates to compute at least one of phase error and frequency error.

21. (Currently Amended) The integrated circuit synchronous read channel of claim 10, wherein the timing recovery circuit ~~computes~~ operates to compute timing error at transition times.

22. (Currently amended) The integrated circuit synchronous read channel of claim 9 wherein the digital pulse shaping filter circuitry ~~includes~~ comprises variable filter parameters.

23. (Currently amended) The integrated circuit synchronous read channel of claim 9

wherein the digital pulse shaping filter circuitry ~~includes~~ comprises programmable filter parameters.

24. (Currently Amended) The integrated circuit synchronous read channel of claim 9 further comprising spectrum smoothing filter circuitry ~~for filtering~~that operates to filter the digitized read signals prior to processing by the sequence detector.

25. (Currently Amended) The integrated circuit synchronous read channel of claim 14, wherein the sequence detector ~~allows~~ operates to allow selection between center and side sampling of the digitized read signals.

26. (Currently Amended) The integrated circuit synchronous read channel of claim 14, wherein the sequence detector ~~accommodates~~ operates to accommodate pulse asymmetry in the digitized read signals.

27. (Previously presented) The integrated circuit synchronous read channel of claim 14, wherein the sequence detector is a partial response sequence detector.

28. (Previously presented) The integrated circuit synchronous read channel of claim 14, wherein the timing recovery circuit operates in at least one of an acquisition mode and a tracking mode.

29. (Previously presented) The integrated circuit synchronous read channel of claim 14, wherein the timing recovery circuit is programmable.

30. (Currently Amended) The integrated circuit synchronous read channel of claim 14, wherein the timing recovery circuit ~~computes~~ operates to compute at least one of phase error and frequency error.

31. (Currently Amended) The integrated circuit synchronous read channel of claim 14, wherein the timing recovery circuit ~~computes~~ operates to compute timing error at transition times.